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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/759,690	01/16/2004	Richard L. Black	P/10-658	8450
2352	7590	10/20/2006	EXAMINER	
OSTROLENK FABER GERB & SOFFEN 1180 AVENUE OF THE AMERICAS NEW YORK, NY 100368403			ROMAN, LUIS ENRIQUE	
			ART UNIT	PAPER NUMBER
			2836	

DATE MAILED: 10/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/759,690

Applicant(s)

BLACK, RICHARD L.

Examiner

Luis Roman

Art Unit

2836

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 July 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-14 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____.

- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date: _____.
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____.

DETAILED ACTION

Applicant amendment filed on 07/17/06 has been entered. Accordingly claims 3-8, 11-14 have been kept original, claims 1, 2, 9, 10 have been amended and no claims have been cancelled. No new claims were added. It also included remarks/arguments.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

102(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 3, 7, 8, 9, 10, 13 & 14 are rejected under 35 U.S.C. §102(b) as being anticipated by Makaran (US 6630805).

Regarding claim 1 Makaran discloses an overcurrent protection circuit for a power switching transistor wherein the power switching transistor (Fig. 2 element S<L represents the load which may be a motor>) has a control electrode (implicitly disclosed any electronic switch has a control electrode<examples MOSFET: gate & BIPOLAR: base) and two main electrodes (Fig. 2 connections to L & GROUND), the circuit comprising: a sensing circuit including a protection switch (Col. 1 lines 23-31 & Fig. 29 elements L, 54, C <comprising an snubber>) for sensing the rate of change of voltage with respect to time at one of the main electrodes of the power switching transistor (Fig. 2 element C) and for controlling the protection switch (Fig. 29 elements 54) to remove a control signal to the control electrode of the power switching transistor to turn off the power switching transistor if the rate of change exceeds a first predefined value the predefined value is inherent with the chosen components of the snubber (Cols. 6 lines 35-45, 7 lines 16-23).

Note: a snubber is a device, which senses and suppresses voltage transients - dv/dt.

Regarding claim 2 Makaran discloses the circuit of claim 1.

Makaran further discloses wherein the sensing circuit comprises a capacitor (Fig. 2 element C) coupled to a main electrode of the power switching transistor (Fig. 2 element S coupled to C) and a resistor (Fig. 2 element R) coupled to receive a pulse of current from said capacitor, such that a voltage developed across the resistor turns on the protection switch if the voltage across the resistor exceeds a second predefined value (Cols. 6 lines 35-45, 7 lines 16-23).

Regarding claim 3 Makaran discloses the circuit of claim 2.

Makaran further discloses wherein the protection switch comprises a transistor (Fig. 29 element 54).

Regarding claim 7 Makaran discloses the circuit of claim 3.

Makaran further disclose wherein the protection switch comprises a field effect transistor JFET (Fig. 29 element 54).

Regarding claim 9 Makaran discloses an overcurrent protection circuit for a power switching transistor wherein the power switching transistor (Fig. 2 element S<L represents the load which may be a motor>) has a control electrode (implicitly disclosed any electronic switch has a control electrode<examples MOSFET: gate & BIPOLAR: base) and two main electrodes (Fig. 2 connections to L & GROUND), the circuit comprising: a protection transistor (Fig. 29 elements 54), and an R-C circuit (Fig. 2 elements R, C) for sensing the rate of change of voltage with respect to time at one of the main electrodes of the power switching transistor (Fig. 2 element VA) and for controlling the protection transistor (Fig. 29 elements 54) to remove a control signal to the control electrode of the power switching transistor to turn off the power switching transistor if the rate of change exceeds a predefined value (Cols. 6 lines 35-45, 7 lines 16-23).

Regarding claim 10 Makaran discloses the circuit of claim 9. Makaran further discloses wherein the R-C circuit comprises a capacitor coupled to a main electrode of the power switching transistor and a resistor coupled to receive a pulse from said capacitor (Fig. 2 element R, C, VA, S) and for developing a voltage across the resistor to turn on the protection transistor if the voltage across the resistor exceeds the predefined value (Col. 1 lines 23-31 & Cols. 6 lines 35-45, 7 lines 16-23).

Regarding claim 13 Makaran discloses the circuit of claim 10. Makaran further discloses wherein the protection transistor comprises a field effect transistor (JFET) (Fig. 29 element 54).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. §103(a), which forms the basis for all obviousness rejections, set forth in this office action.

A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 4 & 11 are rejected under 35 U.S.C. §103(a) as being unpatentable over Makaran (US 6630805) in view of Archer (US 4365171).

Regarding claims 4 & 11 Makaran discloses the circuit of claims above. Makaran does not disclose wherein the protection switch comprises a bipolar junction transistor. Archer teaches an snubber circuit wherein the protection switch comprises a bipolar junction transistor (Fig. 2 element 10). It would have been obvious to a person with the skill in the art at the time the invention was made to modify the Makaran device with the Archer teachings because provides an

improved snubber circuit for a switching transistor which significantly reduces overshoot voltage (Archer<Col. 1 lines 31-32>).

Claims 5, 6 & 12 are rejected under 35 U.S.C. §103(a) as being unpatentable over Makaran (US 6630805) in view of Archer (US 4365171) and Heminger et al. (US 5751052).

Regarding claims 5, 6 & 12 Makaran in view of Archer discloses the circuit of claims above.

Makaran in view of Archer does not disclose wherein the resistor is coupled across the base-emitter junction of the protection transistor and a diode coupled across the base-emitter junction of the protection transistor to discharge the capacitor.

Heminger et al. teaches wherein the resistor is coupled across the base-emitter junction of the protection transistor (Fig. 1 elements 11, 14) and a diode coupled across the base-emitter junction of the protection transistor to discharge the capacitor (Fig. 1 elements 11, 13).

It would have been obvious to a person with the skill in the art at the time the invention was made to modify the Makaran in view of Archer device with the teachings of Heminger et al. because this configuration protects the transistors against leakage and spikes (Heminger et al.<Col. 1 line 61 to Col. 2 line 5>).

Claims 8 & 14 are rejected under 35 U.S.C. §103(a) as being unpatentable over Makaran (US 6630805) in view of Archer (US 4365171) and Turvey et al. (US 6759835).

Regarding claim 8 & 14 Makaran discloses the circuit of claims above.

Makaran does not disclose wherein the power switching transistor comprises a field effect transistor (FET).

Turvey et al. teaches a control circuit wherein the power switching transistor comprises a field effect transistor (FET) (Fig. 1 element TR1).

Art Unit: 2836

It would have been obvious to a person with the skill in the art at the time the invention was made to modify the Makaran device with the teachings of Turvey et al. because this switches provide a cost effective solution while exhibiting good switching characteristics and low "ON" resistance (Turvey et al.< Col. 2 lines 43-46>).

Applicant's arguments with respect to claims 1-14 have been considered but are moot in view of the new ground(s) of rejection.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luis E. Román whose telephone number is 571-272-5527. The examiner can normally be reached on Mon – Fri from 7:15 AM to 3:45 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2800 x 36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from Patent Application Information Retrieval (PAIR) system.

Status information for unpublished applications is available through private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LR/101506

Luis E. Román
Patent Examiner
Art Unit 2836



BRIAN SIRCUS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800